

1 36232/PBH/B600 (BP 1255)

SYSTEM AND METHOD FOR PROVIDING A LOW POWER RECEIVER DESIGN

5 ABSTRACT OF THE DISCLOSURE

10 An integrated receiver with channel selection and image
rejection substantially implemented on a single CMOS integrated
circuit is described. A receiver front end provides programable
attenuation and a programable gain low noise amplifier. Frequency
conversion circuitry advantageously uses LC filters integrated
15 onto the substrate in conjunction with image reject mixers to
provide sufficient image frequency rejection. Filter tuning and
inductor Q compensation over temperature are performed on chip.
The filters utilize multi track spiral inductors. The filters
are tuned using local oscillators to tune a substitute filter,
and frequency scaling during filter component values to those of
the filter being tuned. In conjunction with filtering, frequency
planning provides additional image rejection. The advantageous
choice of local oscillator signal generation methods on chip is
20 by PLL out of band local oscillation and by direct synthesis for
in band local oscillator. The VCOs in the PLLs are centered
using a control circuit to center the tuning capacitance range.
A differential crystal oscillator is advantageously used as a
frequency reference. Differential signal transmission is
25 advantageously used throughout the receiver.

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